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EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/819,996	BENNETT ET AL.	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17, 19-27, and 30* is/are rejected.

7)☒ Claim(s) *18,28 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the amended portions in claims 3 and 9, which state a threshold value defining a point to fetch data, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 3 and 9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The amended portion stating a threshold value defining a point to fetch data is not supported by the original presentation.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Neal et al. (U.S. Patent No. 5,774,706).

Referring to claims 1 and 21: Neal discloses a system memory/DRAM (figure 1, structure 106) connected to the PCI bridge/memory controller (figure 1, structure 110). Neal discloses that a ground pin is utilized in the PCI bus to determine the bus operating frequency (column 2, lines 12-24). Thus, the data fetching from the DRAM to the PCI devices via the bridge based on

the determination on whether the ground pin is grounded is the claimed **obtaining parameters relating data fetching from said memory component based on an operating frequency of a bus.** And the actual data fetching is the claimed **fetching said data from said memory component based on said obtained parameters**. Hence, claim is anticipated by Neal.

5. Claims 1, 21, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Kelley et al. (U.S. Patent No. 6,295,568).

Referring to claims 1 and 21: Kelley discloses a system supporting multiple frequencies. Kelley discloses a system memory (figure 3, structure 50) and frequency control logic within the PCI bridge (figure 3, structure 76). Kelley's frequency control logic determines the frequency by polling the PCI peripheral component slots. Thus, the data fetching from the system memory to the PCI device via the PCI bridge based on the frequency controlled by the frequency control logic is the clamed **obtaining parameters relating data fetching from said memory component based on an operating frequency of a bus.** And the actual data fetching is the claimed **fetching said data from said memory component based on said obtained parameters**. Hence, claim is anticipated by Kelley.

Referring to claim 24: Claims 1 and 21's arguments apply; furthermore, Kelley discloses the parameter set (clock speed, column 1, line 62, loading effect, column 4, 1st paragraph) from a plurality of parameter sets.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Neal and Avery et al. (U.S. Patent No. 5,577,213) or the combination of the Kelley and Avery.

Referring to claim 2: Neal's disclosure is stated above. Neal discloses that the PCI bus can support multiple frequencies, but Neal does not disclose any interface implementation in responding to the frequency change. Kelley's disclosure is stated above. Kelley discloses a plurality of PCI bus regions with different frequencies to support different PCI devices. Kelley discloses a PCI bridge connecting to each of the bus segment with different PCI frequencies, but Kelley does not disclose or teach any special interface to support different frequencies.

Avery discloses a customized interface accepting configuration parameters. Avery teaches one to configure the interface buffers in different sizes in responding to the given system

constraint, such as the bus latency (column 9, lines 53-57, column 10, lines 6-12). Avery further factors the cache line size into the interface customization (column 10, line 9). The cache line size is the transfer size.

Thus, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Avery's teaching onto Neal or Kelley because Avery teaches one a dynamic interface to support different bus frequencies and to accommodate dissimilar devices by setting different parameters to obtain the optimum system efficiency.

Referring to claim 3: Avery disclosed the almost full and almost empty flags (column 9, line 59), which are the threshold values.

Referring to claim 4: Avery discloses registers for storing the parameters/configuration information (column 15-16, table 1).

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the combination of Kelley and Avery, and PCI Specification by the PCISIG.

Referring to claim 5: Claims 1 and 3's rejections apply. Kelley discloses the PCI standard; thus, one with ordinary skill in the computer art will seek the PCI standard to implement the invention. The PCI standard discloses a plurality of data phases in a data transmission (page 36, figure 3-1), which is the claimed initial amount of data and the additional amount of the data during the data transmission.

10. Claims 5-6 are also rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the combination the Kelley and Chambers et al. (U.S. Patent No. 6,289,406).

Referring to claim 5: Kelley's disclosure is stated above. Kelley does not disclose details of the data transmission. Chamber discloses a method to optimize the performance of a bus bridge. Chambers discloses a bridge with a memory component (figure 3, structure 304) and a storage device (figure 4, structure 330 or structure 322). Chambers discloses asserting access request (figure 6, step 505), which is the claimed fetching an initial amount of data from said memory component and storing said initial amount of data in a storage device. Chambers further discloses forwarding data with latency (figure 6, steps 521-540), which is the claimed fetching-additional data from said memory component at least based on a threshold value of said storage device.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Chamber's teaching onto Kelley because Chamber teaches one to optimize the system performance by enabling one to minimize the unnecessary access retries between the initiator device and the bus bridge and to reduce the consequences of repeated access attempts from clogging the bus bandwidth.

Referring to claim 6: Chamber discloses a timer communicating the delayed latency period to the PCI target (column 7, lines 56-57). Chamber further discloses that the PCI target will not retry the access for the period of the time (column 7, lines 59-60). Therefore, Chamber discloses the PCI target will retry the access after the delayed period of time communicated from the timer, and the retry behavior is equivalent to the claimed date fetching. Thus, Chamber discloses fetching data when a timer has elapsed.

11. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the combination of Kelley and Avery, PCI Specification by the PCISIG, and Brown (U.S. Patent No. 6,728,808)

Referring to claim 6: The PCI standard discloses the retry behavior, but none of Kelley, Avery, and PCI standard discloses a timer. Brown discloses that since the PCI specification dictates that only one transaction can take place over the PCI bus at any given time, the PCI bus can be tied up by a PCI bus master continually reissuing the transaction request (column 2, lines 24-30). Brown discloses a retry timer circuit to dynamically control the transaction retries issued by a PCI bus master to a target device; Brown further discloses a latency determination circuit to determine a delay value (column 3, lines 9-12 and 20-22). Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Brown's teaching onto Kelley and Avery because Brown teaches one to use a retry timer and a latency determination circuit to prevent the PCI bandwidth from been occupied by continuously retry request.

12. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the combination of Kelley and Avery.

Referring to claim 7: Kelley's disclosure is stated above. Kelley discloses a system supporting multiple frequencies. Kelley further discloses a frequency control logic, which determines the frequency by polling the PCI peripheral component slots; the control logic is the clamed **control unit to receive an indication regarding a frequency of a bus.** Kelley discloses a PCI bridge connecting to each of the bus segment with different PCI frequencies, but Kelley

does not disclose or teach any special interface to support different frequencies. Avery discloses a customized interface accepting configuration parameters to obtain optimized efficiency. Avery teaches one to configure the interface buffers in different sizes in responding to the given system constraint, such as the bus latency (column 9, lines 53-57, column 10, lines 6-12). Avery discloses registers for storing the parameters/configuration information (column 15-16, table 1).

Thus, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Avery's teaching onto Kelley because Avery teaches one a dynamic interface to support different bus frequencies and to accommodate dissimilar devices by setting different parameters to obtain the optimum system efficiency.

Referring to claim 8: Avery discloses a customized interface between the bus and peripheral device, which the interface accepts the parameters for configuration. Avery teaches one to configure the buffers in different sizes (column 10, lines 6-12).

Referring to claim 9: Avery disclosed the almost full and almost empty flags (column 9, line 59), which are the threshold values.

13. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Chambers, Kelley, and Avery.

Referring to claim 10: Chambers discloses a bridge with a memory component (figure 3, structure 304) and a storage device (figure 4, structure 330 or structure 322). Chambers discloses asserting access request (figure 6, step 505), which is the claimed fetching an initial amount of data from said memory component and storing said initial amount of data in a storage device. Chambers further discloses forwarding data with latency (figure 6, steps 521-540),

which is the claimed fetching-additional data from said memory component at least based on a threshold value of said storage device.

Chambers does not explicitly disclose multiple frequencies. Kelley discloses a system supporting multiple frequencies of different devices. Kelley discloses that a memory component, such as the PCI hard drive, is well known in a computer system (column 1, lines 34-36). Kelley further discloses a frequency control logic, which determines the frequency by polling the PCI peripheral component slots; the control logic is the clamed **control unit to receive an indication regarding a frequency of a bus.**

Kelley discloses a PCI bridge connecting to each of the bus segment with different PCI frequencies, but Kelley does not disclose or teach any special interface to support different frequencies. Kelley's bridge uses switches to connect and disconnect each bus segment. Avery discloses a customized interface accepting configuration parameters to obtain optimized efficiency. Avery discloses registers for storing the parameters/configuration information (column 15-16, table 1). Avery teaches one to configure the buffers in different sizes (column 10, lines 6-12).

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Kelley and Avery's teachings onto Chambers because Kelley teaches one to dynamically adjust the bus frequency to optimize the bus performance and Avery teaches one to enable a bus to accommodate dissimilar devices by setting different parameters.

Referring to claim 11: Kelley, Avery, and Chamber's disclosures are stated above. Furthermore, Chamber discloses a timer communicating the delayed latency period to the PCI

target (column 7, lines 56-57). Chamber further discloses that the PCI target will not retry the access for the period of the time (column 7, lines 59-60). Therefore, Chamber discloses the PCI target will retry the access after the delayed period of time communicated from the timer, and the retry behavior is equivalent to the claimed date fetching. Thus, Chamber does disclose fetching data when a timer has elapsed.

14. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Kelley and Chambers.

Referring to claim 12: Chambers discloses fetching a size of data from a memory subsystem on one side of a host chipset (figure 4, structure 306) for a bus device on an opposite side of said host chipset as a function of said frequency of said bus.

Referring to claim 13: Chambers discloses a primary bus and a secondary bus (figure 4, structures 310 and 312).

Referring to claim 14: Chambers discloses the bus as PCI bus and the chip-set as the PCI bridge. Kelley discloses a PCI-to-PCI bridge (figure 3, structure 76, abstract).

15. Claims 15-17 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Chambers, Kelley, and Avery.

Referring to claim 15: Chambers discloses a memory subsystem (figure 4, structure 304), host chipset (figure 4, structure 306) couple to the memory subsystem via a first bus (figure 4, structure 310), and a bus device (figure 4, structure 330) to couple to said host chipset via a second bus (figure 4, structure 312). Chambers further discloses that the host chipset fetches

data from said memory subsystem for said bus device upon request (figure 6), said host chipset comprising, a buffer device (figure 4, structure 322) to store data fetched from said memory subsystem via said first bus for said bus device.

Chambers does not explicitly disclose a plurality of registers each to contain parameters corresponding to a different operating frequency of said second bus and a data fetching mechanism to receive an indication of an operating frequency of said second bus and to obtain said parameters corresponding to said operating frequency of said second bus based on said indication, fetch said data from said memory component based on said obtained parameters.

Kelley discloses a system supporting multiple frequencies. Kelley discloses that a memory component, such as the PCI hard drive, is well known in a computer system (column 1, lines 34-36). Kelley further discloses a frequency control logic, which determines the frequency by polling the PCI peripheral component slots; such polling is the clamed **obtaining parameters relating data fetching from said memory component based on an operating frequency of a bus.** And the actual data fetching is the claimed **fetching said data from said memory component based on said obtained parameters**.

Although Kelley discloses multiple frequencies, Kelley does not explicitly disclose how to track each bus frequency region's parameters. Avery discloses registers for storing the parameters/configuration information (column 15-16, table 1). Avery teaches one to configure the buffers in different sizes (column 10, lines 6-12).

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Kelley and Avery's teaching onto Chambers because Kelley teaches one to dynamically adjust the bus frequency to optimize the bus performance and

Avery teaches one to enable a bus to accommodate dissimilar devices by setting different parameters.

Referring to claim 16: Chambers discloses a PCI bridge, and the PCI standard specifies it to be either 32 or 64 bits (Application, page 1, last line).

Referring to claim 17: Kelley discloses a PCI-to-PCI bridge (figure 3, structure 76, abstract).

Referring to claim 19: Chambers discloses asserting access request (figure 6, step 505), which is the claimed fetching an initial amount of data from said memory component and storing said initial amount of data in a storage device. Chambers further discloses forwarding data with latency (figure 6, steps 521-540), which is the claimed fetching-additional data from said memory component at least based on a threshold value of said storage device.

Referring to claim 20: Kelley, Avery, and Chamber's disclosures are stated above. Furthermore, Chamber discloses a timer communicating the delayed latency period to the PCI target (column 7, lines 56-57). Chamber further discloses that the PCI target will not retry the access for the period of the time (column 7, lines 59-60). Therefore, Chamber discloses the PCI target will retry the access after the delayed period of time communicated from the timer, and the retry behavior is equivalent to the claimed date fetching. Thus, Chamber does disclose fetching data when a timer has elapsed.

16. Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Kelley and Chambers.

Referring to claim 22: Kelly's disclosure is stated above. Kelly does not disclose details of the data transmission. Chamber discloses a method to optimize the performance of a bus bridge. Chambers discloses a bridge with a memory component (figure 3, structure 304) and a storage device (figure 4, structure 330 or structure 322). Chambers discloses a system memory component (figure 3, structure 304) and a storage device (figure 4, structure 330 or structure 322). Chambers discloses asserting access request (figure 6, step 505), which is the claimed fetching an initial amount of data from said memory component and storing said initial amount of data in a storage device. Chambers further discloses forwarding data with latency (figure 6, steps 521-540), which is the claimed fetching additional data from said memory component at least based on a threshold value of said storage device.

Referring to claim 23: Kelley, Avery, and Chamber's disclosures are stated above. Furthermore, Chamber discloses a timer communicating the delayed latency period to the PCI target (column 7, lines 56-57). Chamber further discloses that the PCI target will not retry the access for the period of the time (column 7, lines 59-60). Therefore, Chamber discloses the PCI target will retry the access after the delayed period of time communicated from the timer, and the retry behavior is equivalent to the claimed date fetching. Thus, Chamber does disclose fetching data when a timer has elapsed.

17. Claims 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the combination of Kelley and Avery.

Referring to claim 25: Kelley's disclosure is stated above. Kelly discloses a plurality of PCI bus regions with different frequencies to support different PCI devices. Kelly discloses a

PCI bridge connecting to each of the bus segment with different PCI frequencies, but Kelly does not disclose or teach any special interface to support different frequencies. Avery discloses a customized interface accepting configuration parameters to obtain optimized efficiency. Avery teaches one to configure the interface buffers in different sizes in responding to the given system constraint, such as the bus latency (column 9, lines 53-57, column 10, lines 6-12). Avery further factors the cache line size into the interface customization (column 10, line 9). The cache line size is the transfer size. Thus, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Avery's teaching onto Kelley because Avery teaches one a dynamic interface to support different bus frequencies and to accommodate dissimilar devices by setting different parameters to obtain the optimum system efficiency.

Referring to claims 26-27: Avery disclosed the almost full and almost empty flags (column 9, line 59), which are the threshold values. Avery's flags identify the current status of the capacity of the data transmission and then to issue another request accordingly. Avery also discloses buffer for the data transmission (figure 5, structures 22).

18. Claims 26-27, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Kelley and Chambers.

Referring to claims 26-27: Kelley's disclosure is stated above. Kelly does not disclose details of the data transmission. Chamber discloses a method to optimize the performance of a bus bridge. Chambers discloses a bridge with a memory component (figure 3, structure 304) and a storage device (figure 4, structure 330 or structure 322). Chambers discloses fetching

comprises issuing a request to transfer data from the memory component to a buffer, and then issuing another request in response to the threshold value and a data amount comprising data stored in the buffer indicating that more data needs to be fetched to maintain a stream of data between the buffer and a device (figure 4, structures 322, 324, and 330).

Referring to claim 30: Chambers discloses fetching said data further comprises starting a timer, and fetching additional data from said memory component when said timer has elapsed (figure 4, structure 324, column 7, lines 56-61).

Response to Arguments

19. In response to Applicant's argument that Neal does not disclose fetching data from a system memory (Remark, page 11, 3rd paragraph, page 12, 1st paragraph): Neal does disclose a system memory/DRAM (figure 1, structure 106) connected to the PCI bridge/memory controller (figure 1, structure 110). Neal discloses that a ground pin is utilized in the PCI bus to determine the bus operating frequency (column 2, lines 12-24). Thus, the data fetching from the DRAM to the PCI devices via the bridge based on the determination on whether the ground pin is grounded is the claimed **obtaining parameters relating data fetching from said memory component based on an operating frequency of a bus.** And the actual data fetching is the claimed **fetching said data from said memory component based on said obtained parameters**. Hence, claim is anticipated by Neal.

20. In response to Applicant's argument that Avery provides no teaching in regard to obtaining a data transfer size based upon the operating frequency of the bus (Remark, page 14, 2nd paragraph, page 16, 1st paragraph): Both Kelley and Neal disclose a PCI bus system with

multiple frequencies, but neither discloses or teaches any special interface to support or to optimize the different frequencies. Avery teaches one to configure the interface buffers in different sizes in responding to the given system constraint, such as the bus latency and overhead (column 9, lines 53-57, column 10, lines 6-12). The bus latency and the bus frequency are closely related. Avery further factors the cache line size into the interface customization (column 10, line 9). The cache line size is the transfer size.

21. In response to Applicant's argument that Avery does not disclose the registers for storing bus frequencies as claimed in the claim 4 (Remark, page 15, 2nd paragraph, last 3 lines): Claim 4 is rejected by the combination of the Kelley and Avery. As disclosed by the Kelley, the registers are known to store the configuration information, such as the range registers in the PCI bridge's control logic (figure 3, structure 76). While Kelley discloses a plurality of bus frequencies, Kelley does not disclose or teach any special interface to support or to optimize the different frequencies. Avery teaches one to customize the interface to optimize the data transmission, and Avery's customized interface accepts configuration parameters for optimized efficiency. Avery teaches one to configure the interface buffers in different sizes in responding to the given system constraint, such as the bus latency (column 9, lines 53-57, column 10, lines 6-12); Avery further discloses registers for storing the parameters/configuration information (column 15-16, table 1). It is the Avery's teaching that registers are used in storing the customized interface's parameters. Kelley's invention's different bus frequencies are a part of the bus latency/system constraint factor as taught by Avery. Hence, one with ordinary skill in the computer art will factor Kelley's multiple bus frequencies into the interface customization and store the related information in the parameter registers.

22. In response to Applicant's argument that Avery's buffer widths would not be viewed as the threshold value (Remark, page 14, last paragraph) and Avery does not teach fetching data based on a threshold value (Remark, page 20, 1st paragraph): Avery disclosed the almost full and almost empty flags (column 9, line 59), which are the threshold values. The almost full and almost empty flags are used as referencing to fetch data.

23. In response to Applicant's argument that Avery does not teach obtaining the parameters from a register that corresponds to the bus frequency (Remark, page 15, 2nd paragraph): Avery teaches one to configure the interface buffers in different sizes in responding to the given system constraint, such as the bus latency and overhead (column 9, lines 53-57, column 10, lines 6-12). The bus latency is related to the bus frequency.

24. In response to Applicant's argument that Chambers does not disclose fetch data when a timer has elapsed (Remark, page 18, last paragraph, page 19, last paragraph); Applicant argues that Chamber stops a data transfer when it has elapsed by relinquishing the bus (Remark, page 19, line 3): Chamber discloses a timer communicating the delayed latency period to the PCI target (column 7, lines 56-57). Chamber further discloses that the PCI target will not retry the access for the period of the time (column 7, lines 59-60). Therefore, Chamber discloses the PCI target will retry the access after the delayed period of time communicated from the timer, and the retry behavior is equivalent to the claimed date fetching. Chamber's timer does not stop the data transfer; Chamber's timer delays the PCI device's retry attempt. Thus, Chamber does disclose fetching data when a timer has elapsed. In addition, the Office Action above has added another prior art Brown for the teachings of a delay timer.

Allowable Subject Matter

25. Claims 18 and 28-29 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Referring to claim 18: The prior arts on record do not disclose or explicitly teach initial request length, initial threshold length, subsequent request length, and subsequent threshold length as the parameters relating to data fetching based on the operating frequency of the bus.

Referring to claim 28: The prior arts on record do not disclose or explicitly teach that each parameters set includes a first data transfer size and a second data transfer size, and system fetches a first request to request data having the first data transfer size and issues the second request to request data having the second data transfer size.

Referring to claim 29: The prior arts on record do not disclose or explicitly teach that each parameter set includes a first data transfer size, a second data transfer size, a first threshold value, and a second thresh based upon corresponding operating characteristics of the bus. The prior arts on record also do not disclose or explicitly teach that fetching a first request to transfer data having the first data transfer size from the memory component to a buffer, issuing a second request to transfer data having the second data transfer size from the memory component to the buffer.

Conclusion

26. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP§706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 571-272-3628. The examiner can normally be reached on Monday through Friday, 9:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Justin King
February 13, 2005